A Critical Review on VLSI Architectures for Analog to Digital Converters

Meena Prasad[1], Ajay Barapate[2]
[1,2]*Department of ECE, Vedica Institute of Technology, RKDF University, Bhopal, M.P*
[1]*mprasad097@gmail.com*, [2]*barapatre.ajay@yahoo.com*

Abstract: ***A series of recent studies has indicated that a mixed signal device analog to digital converters used for the processing of information and play a vital role in wireless sensors, Digital signal processing, Biomedical devices, in communication, IOT and various other applications. Across this broad use they give the significance in designing. The paper represents the various parameters like speed, area occupied, power consumption, sampling Rate, precision, Signal to noise ratio, Signal to noise distortion ratio, resolution, linearity and conversion time with respect to its different types and broad application in the real world. It defines errors due to non – linearity of signals as Differential nonlinearity, Integral nonlinearity, gain error, quantization error, aliasing and offset error. It also gives the comparative study about ADCs.***

Keyword:- Analog to digital converters (ADC), sampling rate, power consumption, conversion rate, resolution, errors.

I. INTRODUCTION

In this real world, signals are distinguished as Analog and digital. ADCs are the basic building blocks which define the interfacing link between analog and digital [10]. Also it is defined as important mixed signal device which limits the performance of whole system. ADC converts analog continuous signals to digital discrete time signal [20]. The signal is firstly given to an anti-aliasing filter to remove any high frequency components that may cause the effect called as aliasing [18]. Then signal is sampled, quantized and converted in to discrete signals and at the end low pass filter is used to return analog signal with phase shift.

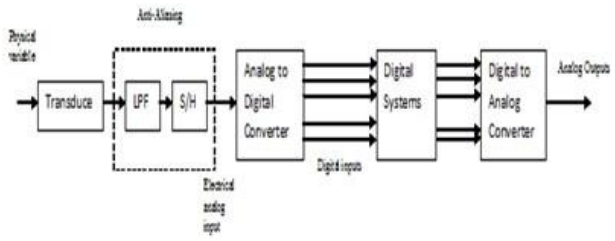


Fig. 1. Basic ADC Diagram

The mixed signal device may be implemented using different performance parameters in many ways[18]. These performance parameters are resolution, speed, power consumption, conversion time, geometry, noise sampling rate etc. which are categorized in static and dynamic characteristics.

II. ANALOG TO DIGITAL CONVERTERS ARCHITECTURES

All ADCs exist with changes in resolutions, Bandwidth, Precision, speed, conversion time and other specifications. The most popular ADC architectures[17] available are flash or parallel comparator ADC, successive approximation ADC, Delta Sigma ADC, n-stage pipelined ADC, Integrating ADC with single slope and multi slope architecture. Nyquist rate ADC and Oversampling ADCs are the types on the basis of sampling rate..

A. Flash ADC:-

If input data is converted into N-Bit digital output word then flash ADC type of architecture is required with 2^N-1 comparators[1] that compare varying reference signal with fixed input signal. The output value of comparator depends on the value of difference between input and reference signal. If input voltage is greater than reference voltage, then output of comparator is '1' otherwise '0'. The reference voltage is given by 2^N division values and each value is given to every comparator. Flash ADC is popular for its fastest speed. So it can be used for very large Bandwidth [9] applications like in Radar Processing [5] hard density disk drives, oscilloscopes. Due to its Parallel architecture of comparators [31] flash ADC is also called as Parallel ADCs [27]. It uses no clock Signal.

Its performance parameter resolution depends on number of comparators used in its architecture [7]. If there is large number of comparators used according to which its Resolution increase [17]. For 6 Bit flash ADC, 63 comparators are required. Similarly for 10 bit it required 1023 comparators [31]. Each comparator is having its own reference voltage which is provided externally [34]. Other Input of each comparator is same i.e., the analog input so that each and every comparator gives output in one cycle. For advancement in the features of flash ADC, another form of flash ADC used known as two step Flash ADCs with feed forward circuitry. It use two ADCs, one for sampling of input signal and other is used to produce least significant bits by flash conversion. The numbers of comparators used in two step converter are very much less than flash converters. It uses residue amplifier and summer amplifier for process of conversion. The conversion process completed in two steps of conversion i.e., coarse and fine conversion. If coarse conversion is not performed properly then it resulted very high error in fine conversion. Hence the accuracy of this converter depends on resistor matching and comparators in first ADC.

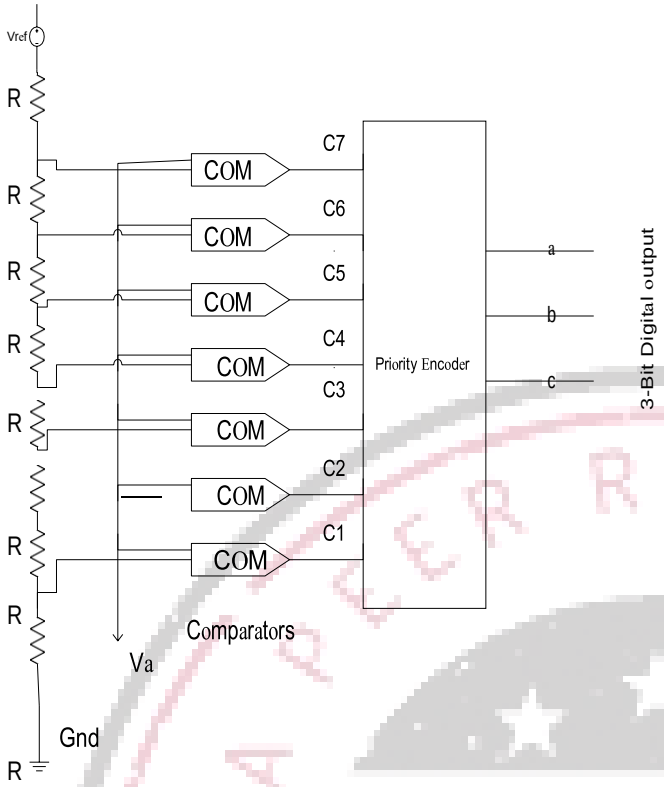


Fig. 2. Flash Analog to Digital Converter

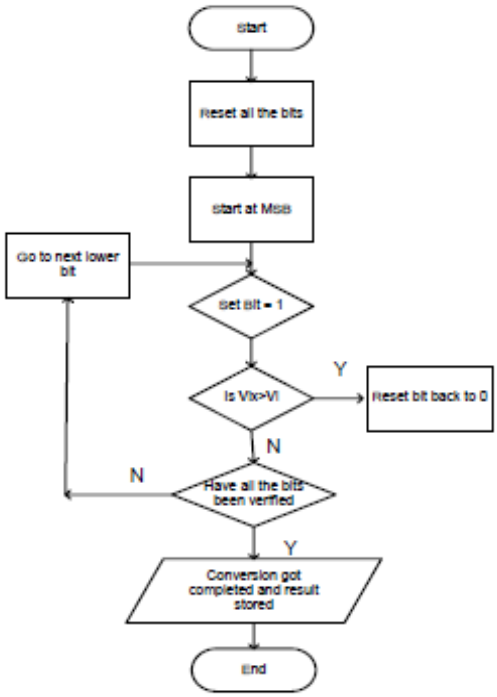


Fig. 3. Flowchart for the operation of SAR - ADC

B. SAR-ADC Architecture:-

SAR is the most important analog to digital converter [35] used in applications that require a sampling rate[5][37] under 10 mSps with resolution 8-16 bits [2]. The operation of SAR-ADC[38] can be easily explained by using following flowchart [11].

In this operation the conversion time vary according to number of bits present in the digital result. Its architecture consist of comparator, control circuit[39], control register [23], DAC and Buffer Register [10]. On the basis of comparator's Output, SAR-ADC logic determines the digital output code that is stored in buffer Register [34]. Its control register [7] contains shift Register[40] also that performs on output value of comparator [11][27]. Initially bits of DAC converter enable '1' at a time beginning with MSB then comparator produce output. If the output of comparator is '0' control logic gives '0'. Then again set MSB as '1' this process continues until all bits of DAC have been tried[34][23]. As conversion process completes, the control circuit sends low signal EOC[11]. Conversion speed is up to 10 Mega samples and resolution is up to 20 bits. Conversion time conversion time[28] is independent of input voltage.Conversion time $t_{conversion} = N*t_{clock}$

SAR – ADC is having very popular binary weighted capacitor array type or charge distribution ADC. This converter type used to perform operation on the basis of amount of charge on each capacitor. This converter is used to perform automatic offset cancellations.

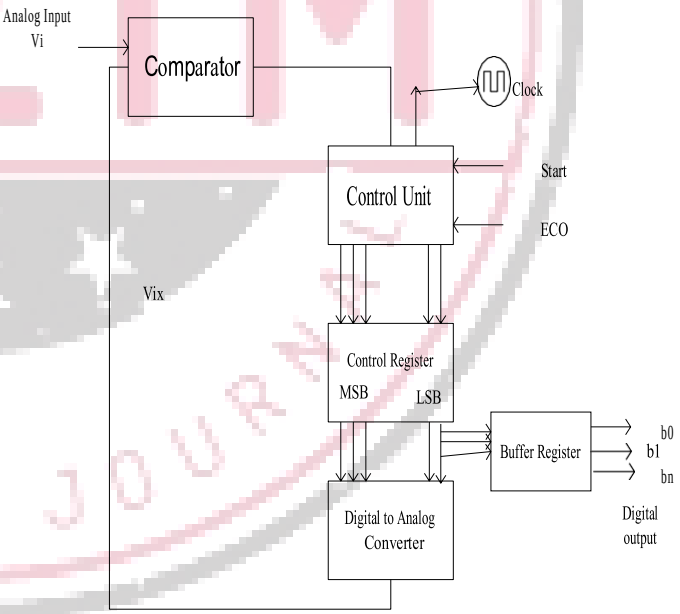


Fig. 4. Successive Approximation Analog to Digital Converter

C. Pipelined ADC

In this we define an application like video, Radar Communication with high speed that is served by a pipelined ADC [6][7]. High resolution and high speed [42][28] are the important features of pipelined ADC. Pipeline ADC [43][26] work on various stages of ADC [34] , its very first stage operates [22] on applied analog input and remaining analog voltages is responsible for the operation of other stages of pipelined ADC[32][27].

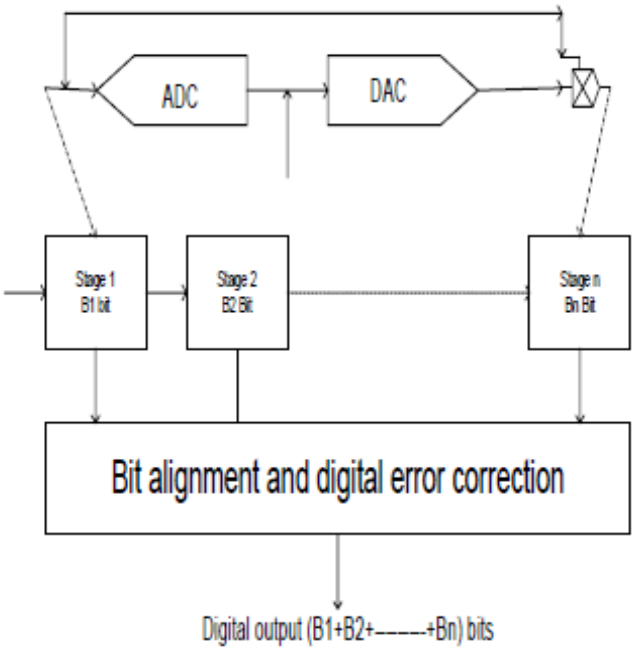


Fig. 5. Pipelined Analog to Digital Converter

D. Sigma Delta ADC

High integration low cost and high resolution[46][47] are important characteristics[5] obtained by using Sigma-Delta ADC's[34]. The Delta ADC consists of Integration, comparator, single Bit DAC, digital filter and decimator[10]. The resultant signal obtained by addition or subtraction of DAC O/P and analog input is applied to integrator[17][18]. Then changes into Bit stream[7] by the application of comparator. Then this Bit stream of data having series of '1' or '0's are filtered at reduced sampling rate[48] using Digital Low Pass filter[27] & Decimator, and resulted Binary format O/P.

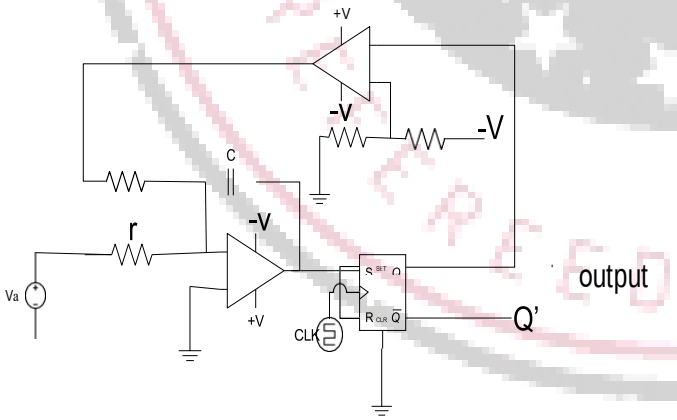


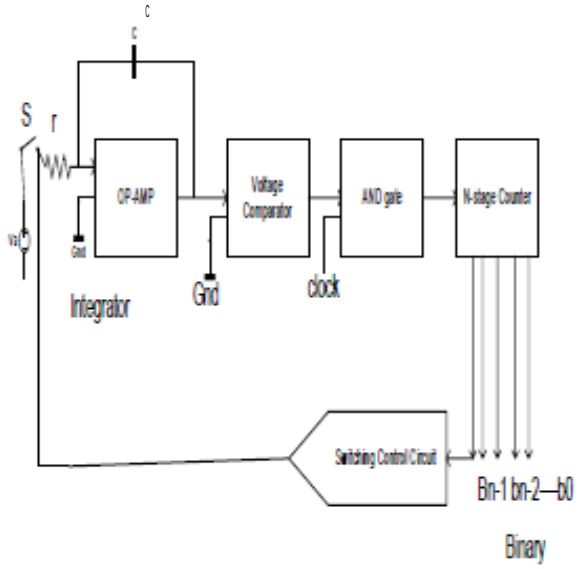
Fig. 6. Sigma Delta Analog to Digital Converter

E. DUAL SLOPE ADC

This ADC has slowest Conversion type but has low cost and high accuracy[44]. It does not use any precision components. Its architecture is having sub parts an integrator[34], a voltage comparator, a Binary counter and a switching control circuit.

In its operation charging and discharging of capacitor with constant current take place. O/P of integrator[10]

the counter counts from 000 ---------000 to 111-------- 111 when 2^N-1 clock pules are applied. The counter counts the pulses (cycles) until $v_0 < 0$[5][7]. It is used in application like digital meter panel meter[24] and monitoring systems.



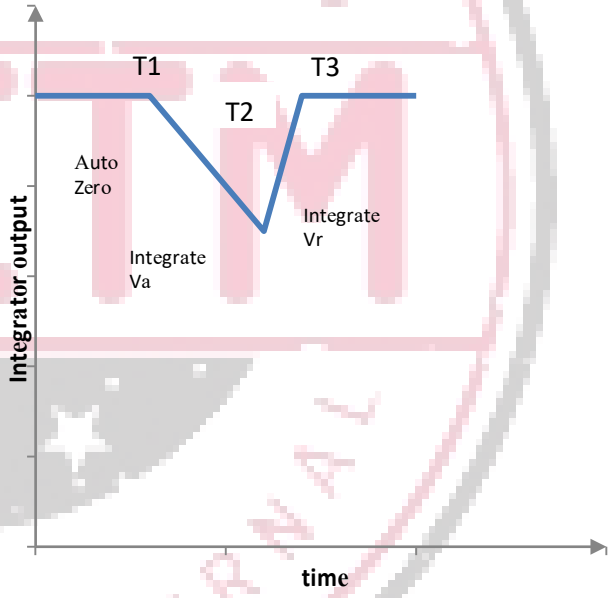


Fig. 7. Dual Slope Analog to Digital Converter and Characteristic

III. PERFORMANCE PARAMETERS

In this section, we discuss the various performance parameters[3] as Resolution, SNR, Linearity, Temperature sensitivity, Precision, Accuracy[28], Power dissipation, conversion time[30], Effective number of Bits (ENOB), sampling rate.

A. Resolution

It is the very smallest change in analog input voltage which may be produced at output with one bit change of converter [18]. Resolution is defined in the form of bits and given as number of input voltage levels i.e., 2^N.

Higher resolution [47][50] is responsible for slower conversion Rate. In flash converters, if the resolution increases by 1-bit, the open loop gain becomes double.

B. Linearity

It is the measure of the precision with which the linear Input-Output relationship is satisfied Linearity [9] depends on the accuracy of the resistors. It may be adverse affected by temperature changes.

C. Temperature Sensitivity

Accuracy of the device depends on temperature[14]. The application of various sensors depends on temperature range.

D. Precision

It describes reproducibility of measurement.

E. Accuracy: - It is defined as the difference between practical value and true value. It is the amount of uncertainty in a measurement w.r.t. absolute standard.

F. SNR and SNDR

Signal to noise (SNR) ratio is the relation between the largest value of RMS input signal and RMS noise value.

$$SNR=20\log(\text{———})$$

Where Vin(max) = peak to peak value of sine wave is given as:

$$Vin(max)=\text{——} \quad)$$

And RMS noise value is given by the error signal $QE_{,RMS}$ as

$$V_{noise} = QE_{,RMS} = \text{—}$$

$$SNR=20N\log(2) + 20\log -20\log(2\ )$$

Higher SNR, better the choice of ADCs.

G. Power Dissipation

Power dissipation scales with sampling rate. It is the function of total voltage and current at output end[33]. Low power consumption occurs due to less area occupied.

H. Total Harmonic Distortion (THD)

In the conversion process the measurement of Harmonic distortion present in a signal is called THD [30]. It is the ratio of addition of harmonic components power to the Power fundamental frequency of signal. It is due to non-linearity of ADC [28]. These are undesirable signals at Output stages. It is measured in decibels (*db).*

I. The Effective Number of Bit (ENOB)

It is the measurement of dynamic range of ADC with its associated circuits. SNR or SNDR of ADC is used to determine the effective number of bits [30] used to represent the analog value. It is determined by using SNDR with full scale sinusoidal input signal.

J. Conversion Time

It is the reciprocal of time[16]. It is used to convert each analog input level to its digital output format.

K. Sampling Rate

It is defined as samples per second, sampling Rate is number of O/P samples available per unit time. According to Nyquist Criterion [17] the sampling rate is two times greater than and equal to the maximum frequency present within the analog signal[18].

$$f_{sampling} \geq f_{max}$$

IV. SOURCES OF ERRORS

A. Quantization Error

When input is infinite valued and output be discrete valued type, then the error [29] resulted is known as quantization error[18]. In other words, it is the difference between actual input analog voltage and output staircase voltage.

$$Q.E=V_{input}-V_{outputstaircase}$$

$$V_{outputstaircase} = d.\text{——} = d.\ V_{lsb}$$

Where d= value of digital discrete type output code

V_{lsb} = voltage of 1 lsb in volts.

The below given transfer curve [17] shows the quantization error of ±1/2lsb for ideal ADC.

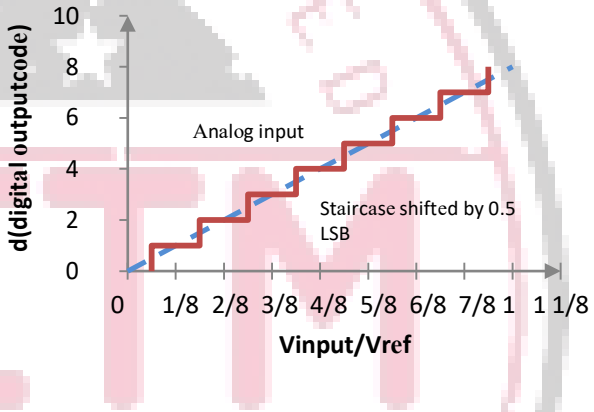


Fig. 8. Characteristic of Digital output code

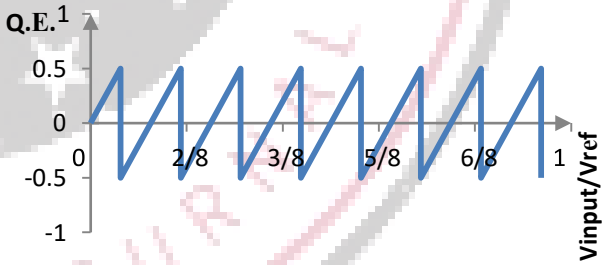


Fig. 9. Quantization Error

B. DNL (Differential Non-linearity)

It is used to describe the changes between two adjacent analog values corresponding to adjacent digital values [18][11]. It defines the difference between actual non ideal code width and ideal case [30].

DNL = Actual non ideal width – Ideal step width

Width value of ideal step of converter is taken as 1/8

$V_{idealstepwidth}=V_{ref}/8$

It gives constant relation between the changes in Input and output.

C. INL (Integral Nonlinearity)

It is measured as the difference between data code converter transition points and reference straight with all remaining errors set to zero[18][16]. In ADCs, it is the change between ideal input threshold value and the measured threshold level of output code[28].

D. Offset Error

It is defined as the difference between first code transition value and ideal value of ½ lsbs. Its value is constant at each and every sample [10][18].

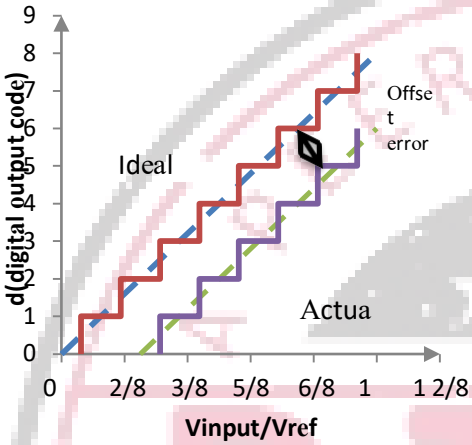


Fig. 10. The Offset Error

E. Gain Error or Scale Factor Error

It is the difference between actual slope of straight line drawn through the transfer characteristics for K<1 and ideal ADC with K=1 [18].

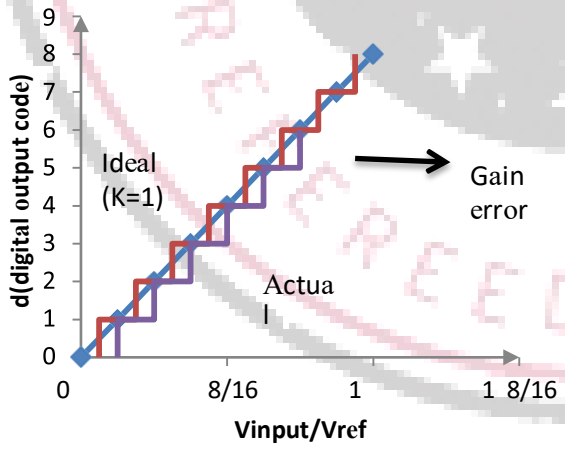


Fig. 11. Gain Error (Scale Factor Error)

F. Aliasing

Aliasing is due to the undersampling[18].

$$F_{aliasing} = f_{actual} + K\, f_{sample}$$

The Aliasing is overcome by sampling with higher frequencies and also by using filtering analog signals before the process of sampling.

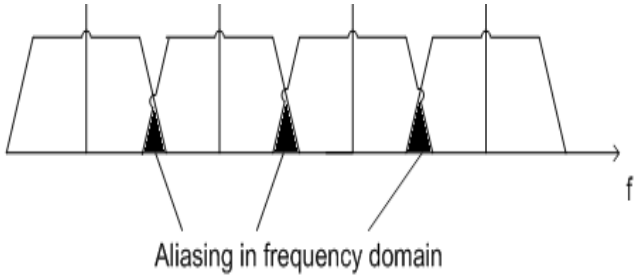


Fig. 12. Aliasing in Frequency Domain

V. APPLICATION OF VARIOUS ADC ARCHITECTURES

ADCs play a vital role in recent application in various fields due to high accuracy, better resolution[17], low power dissipation and better noise immunity features. By increasing speed with use of 3-Bit flash ADC is applicable for wireless LAN applications Image processing. A High degree of comparator is essential for accuracy [26] for good ADC performance. The modern applications Process control, precision temperature measurements and weighing scales are done by using High resolution, high integration with low cost and low Power consumption Delta Sigma Analog to Digital Converters. Dual Slope ADCs are the good choice for measuring temperature transducers. Most commonly used application is digital voltmeters (DVMs). Pipeline ADCs are best known for RF applications Data Acquisition[24][41]. SAR-ADC is used for Bioinformatics and Computational Applications [35]. Also with high speed[42] and lower power dissipation feature of SAR ADC applicable for data acquisition in wireless applications. These ADCs are used for monitoring health in systems using Biopotential Signals [25]. By all these applications, all ADC's architectures are good with their specialty but still there are some comparisons in there architectures on the basis of their performance parameters [29]. Due to high sampling rate, successive approximation analog to digital converters are very much suitable for multiplexed data acquisition used in medical imaging, in multiplexed sensor types like pressure, temperature, load cells [25], industrial process control and optical communication systems. Sigma delta ADC is best applicable for various audio applications. The high speed, low power dissipation, better accuracy and repeatability features make ADCs to suit for machine control and automotive applications. During recent years, the digital still cameras and mobile phone cameras have been used for image sensor applications is possible due to ADCs by considering various parameters. SAR – ADCs are considered as best data loggers, temperature sensors and bridge sensors. High speed pipelined ADCs are very much applicable for measurement and testing the instruments and also in medical imaging systems.

VI. RESULT ANALYSIS

TABLE 1 COMPARISON OF ADCS ON THE BASIS OF PERFORMANCE PARAMETERS

	Flash converter	**Successive approximation converter**	**Dual Slope Integrating**	**n-stage Pipelined**	**Sigma Delta ADC (∑-ADC)**
Resolution (in terms of bits)	Very Low resolution (6 bits - 8 bits)	Medium –high resolution (10 bits -18 bits)	Same as SAR - ADC (12 bits - 18bits)	Medium-high resolution (12 bits - 18 bits)	High resolution (16 bits -24bits)
Sampling rate (samples/sec)	High (1GS/s-10GS/s)	Medium (100KS/s-10MS/s)	Low (100S/s-1000S/s)	Medium-high (10MS/s - 100MS/s)	Low (10KS/s -1MS/s)
Accuracy	Low accuracy	Medium-high	Highly accurate	Medium-high	Medium-high
Conversion time (number of cycles)	1	Variable	$2*2^N$	——	High
Area occupied	Large	Small area occupied	Low	Very large	Medium
Power consumption	Consume high power	Low – ultralow power consumed	Consumed very low power	Very high power consumed	Low consumption
Cost	Expensive	Cheaper	Low cost	Very expensive	Less costly

Fig. 13. Comparison of all types of Analog to Digital Converters

VII. LITERATURE SURVEY

In this paper, ADCs are reviewed by using various techniques of ADCs [7] like successive approximation ADC, Flash/Parallel ADC, Sigma-delta ADC and Dual slope ADC[5]. ADCs have described Gaussian Cummulative distribution function to reduce non-linearity[1][5]. It can seen that increasing number of comparator is responsible for increasing ENOB (Effective number of Bits[1]). This paper [2] defines fundamental operating principal[20] for ADCs architectures with the help of examples, also by considering Design Constraints[3] and draw the comparison of all architectures. ADCs are very important in the interfacing of Analog with the real digital world[4]. A high degree of comparator accuracy is essential for selection of best ADC[15] . There are superior Key design blocks that achieve better performance parameters. This paper defines various parameters like speed, resolution, DNL, INL[7] and static and dynamic Parameters[3]. Sigma delta ADC gives high resolution[5] among ADCs[4]. High resolution with high speed, low power comparators are applied on sample input signals[8] to convert to quantized form. ADCs are very much popular in Digital signal processing applications[7]. On the basis of parameters like Conversion time[4] and Sampling Frequency pipelined ADC[6] are very much used in wireless communication system and portable devices like PC[15] Cellular Phone, Camcorders[6], portable storage devices with low power dissipation due to which High battery life available[9]. Analog to Digital conversion takes basically two techniques to completes its process one is sampling and other is Quantizing.[5] Using Sigma Delta ADCs[10] with different parameters like SNR (Signal to noise ratio) and ENOB that depend on value of order and Quantized[5] Bit Parameters for good Quantization[10] better SNR[3] is required. SAR-ADC with high [9] conversion speed is used to improve conversion error in microcontroller clock. In the real world, Parameters like Pressure, humidity, temperature[11] and voice as analog signal are used in electronic digital techniques. Also, ADCs are time based [12] and voltage based type used for DSP applications. Today, most important application of ADCs is Data Acquisition [18] in Biomedical and in Bioinformatics[25] and in precision industrial measurements. For data acquisition [17] applications SAR-ADC are most popular [18]. In digital oscilloscope and wide band application, optical communication[25], high sampling rate [16] ADCs with medium resolution are required. In this paper comparative study of ADCs take place by analysis of its performance criterions [19] like Power consumption, Resolution and Sampling Rate, ADCs are design by using MOS devices and, Bipolar devices[5].

The objective of Research on ADCs is establish [17] the interface between the sensed environment and sensor network and other performance parameters[16].

VIII. CONCLUSION

Different type of ADCs architectures are studied and analyzed various designing constraints speed, conversion time, sampling Rate, Resolution Power dissipation and Area Occupied. The objective is to design ADCs by using specific technology by which there ADCs are implemented in various applications with low power dissipation and less area occupation.

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